METHOD AND STRUCTURE FOR COMPOSITE TRENCH FILL

This is a divisional of application Ser. No. 10/439,558 filed on May 15, 2003, now U.S. Pat. No. 6,887,768.

FIELD OF THE INVENTION

Embodiments of the present invention relate to the field of silicon electronic devices. In particular, embodiments of the present invention relate to a trench fill method and structure.

BACKGROUND ART

Junction field effect transistors (JFETs) are majority carrier devices that conduct current through a channel that is controlled by the application of a voltage to a p-n junction. JFETs may be constructed as p-channel or n-channel and may be operated as enhancement mode devices or depletion mode devices.

The most common JFET type is the depletion mode type. The depletion mode device is a normally "on" device that is turned off by reverse biasing the p-n junction so that pinch-off occurs in the conduction channel. P-channel depletion mode devices are turned off by the application of a positive voltage between the gate and source (positive V_{gs}), whereas n-channel depletion mode devices are turned off by the application of a negative voltage between the gate and source (negative V_{gs}). Since the junction of a depletion mode JFET is reverse biased in normal operation, the input voltage V_{gs} can be relatively high. However, the supply voltage between the drain and source (V_{ds}) is usually relatively low when the device is switched on.

Enhancement mode, or normally "off" JFETs are characterized by a channel that is sufficiently narrow such that a depletion region at zero applied voltage extends across the entire width of the channel. Application of a forward bias reduces the width of the depletion region in the channel, thereby creating a conduction path in the channel. P-channel enhancement mode JFETs are turned on by the application of a negative V_{gs}, and n-channel enhancement mode JFETs are turned on by the application of a positive V_{gs}. The input voltage of an enhancement mode JFET is limited by the forward breakdown voltage of the p-n junction.

Historically, high voltage applications for transistors have relied chiefly on bipolar junction transistors (BJTs), insulated gate bipolar transistors (IGBTs), and metal oxide semiconductor field effect transistors (MOSFETs). IGBTs and MOSFETs have the disadvantage of being susceptible to gate damage due to static discharge, and BJTs are susceptible to thermal runaway. JFETs do not have these disadvantages. JFETs share the transconductance/temperature behavior of MOSFETs, but they do not rely on an insulated gate.

In the fabrication of silicon electronic devices such as JFETs and MOSFETs, trenches may be etched that require a subsequent fill with a dielectric material. Silicon dioxide is commonly used for trench fill, but there are some disadvantages. As smaller critical dimensions are adopted for the fabrication of silicon electronic devices, thinner layers and finer registration are required, and devices are less tolerant of defects.

With typical oxide deposition processes, voids occasionally form in the region of a filled trench. These voids may form as a result of trench geometry or the characteristics of the oxide deposition process.

Another problem with conventional oxide fills is the difficulty in avoiding the unwanted removal of oxide during subsequent etchback. Unwanted material removal may be the result of over-etching in the vertical dimension or may result from poor lateral registration during an etch step. Shallow trenches are particularly susceptible, since a given amount of over-etching will constitute a greater fraction of the fill. The problem of over-etching of an oxide trench fill may be compounded by a subsequent metal deposition step, resulting in a substitution of metal for a portion of the dielectric oxide fill.

Thus, a need exists for a trench fill method that is capable of reducing the formation of voids in the vicinity of the trench. There is also a need for a trench fill method that protects against oxide over-etching, particularly for shallow trenches.

SUMMARY OF INVENTION

A method and structure for a composite trench fill for silicon electronic devices is disclosed. On a planar silicon substrate having a first deposited layer of oxide and a second deposited layer of polysilicon, a trench is etched. Deposition and etch processes using a combination of oxide and polysilicon are used to fabricate a composite trench fill. The trench bottom and a lower portion of the walls are covered with oxide. The remaining portion of the trench volume is filled with polysilicon. The method may be used for junction field effect transistors (JFETs) and metal oxide semiconductor field effect transistors (MOSFETs).

In an embodiment of the present invention, a planar silicon substrate is prepared by forming a first oxide layer on the surface of the substrate and the subsequent formation of a first polysilicon layer on the first oxide layer. A trench is then etched in the prepared substrate. A second oxide layer is then formed on the substrate and trench surfaces. A second polysilicon layer is deposited over the second oxide layer and etched back so that a polysilicon fill that is approximately level with the surface of the substrate remains within the trench. The second oxide layer is then etched back to produce a gap between the polysilicon fill and the substrate. Finally, a third polysilicon layer is deposited and etched back to fill the gap.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1**A shows a general schematic for an n-channel depletion mode junction field effect transistor (JFET).

FIG. **1**B shows a general schematic for an n-channel enhancement mode junction field effect transistor (JFET).

FIG. **2**A shows a cross-section of a planar silicon substrate prepared for a trench fill in accordance with an embodiment of the present claimed invention.

FIG. **2**B shows the substrate of FIG. **2**A with a second oxide coating in accordance with an embodiment of the present claimed invention.

FIG. **2**C shows the substrate of FIG. **2**B with first polysilicon fills in accordance with an embodiment of the present claimed invention.

FIG. **2**D shows the substrate of FIG. **2**C with the second oxide coating etched back to produce a gap between the substrate and the first polysilicon fill in accordance with an embodiment of the present claimed invention.

FIG. **2**E shows the substrate of FIG. **2**D with second polysilicon fills in accordance with an embodiment of the present claimed invention.